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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/575,298	05/19/2000	Peter Elenius	5833-A-11	1299

7590 07/30/2003

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EXAMINER

PAREKH, NITIN

ART UNIT PAPER NUMBER

2811

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Applicati n No.

09/575,298

Applicant(s)

ELENIUS ET AL.

Examiner

Nitin Parekh

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period of Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 05 May 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 16-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05-19-2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 16 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 16, lines 15 and 19 cite: ".....a mass of low melting temperature reflowable solder having ....".

However, the description in the specification (pages 1-11) does not disclose the solder or the mass of the solder bar being made of a low melting temperature reflowable solder.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negated by the manner in which the invention was made.

4. Claims 16-22 are rejected under 35 U.S.C. 103(a) insofar as in compliance with 35 U.S.C. 112, as being unpatentable over Van Den Brekel et al. (US Pat. 4605153) in view of Amano et al. (US Pat. 5453582) and Dockerty et al. (US Pat. 5796169).

Regarding claim 16, Van Den Brekel et al. disclose a device/package comprising a reflowable hump-shaped solder mass/solder bar formed on an upper surface of a first substrate (10 in Fig. 1 and 2), the substrate having a first electrical contact/pad (11/12 in Fig. 1) and the reflowable solder mass/solder bar being adapted to join the first electrical contact to a second electrical contact on a second substrate (16 in Fig. 2; Col. 2, lines 1-13), the solder mass/solder bar comprising in combination:

- a. a first and second parabolic shaped solder pads (see 12a and 12b defined on a circuit pattern 11 in a plan view of Fig. 1; Col. 1, line 45) formed on the upper surface of the first substrate, the solder pads having length/width dimensions A and B (see Fig. 1)
- b. a central portion of the second solder pad being spaced from that of the first solder pad by a predetermined spacing/distance/BL (not numerically referenced in Fig. 1-see spacing between 12a and 12b in Fig. 1)
- c. a solder bar/solder mass pad of first predetermined width/BW (not numerically referenced in Fig. 1- see width of parallel-sided section 15 connecting 12a and 12b in Fig. 1; Col. 1, line 52) formed on the upper surface of the first substrate connecting the first and second solder pads, the width/BW being less than the dimension B of the solder pad (see Fig. 1)

- d. a mass of reflowable solder having a convex-arcuate humps/bumps (12a and 12b in cross-sectional view in Fig. 2) having a total volume/VB formed on the first and second solder pads to form the reflowable solder mass/solder bar (see shaded area/12 in Fig. 1) reaching a height E/H1 (see Fig. 2) above the centers of the first and second solder pads and a different height/H2 at the midpoint/neck portion (not numerically referenced in Fig. 2- Col. 1, line 54) between the humps of the solder mass/solder bar(16, 18, etc. in Fig. 4), a width of the lowermost base region of the solder mass adjacent the solder bar/solder mass pad being substantially equal to the solder pad width/BW (see Fig. 1), and
- e. values for predetermined solder pad dimensions A/B, spacing/BL, solder pad width/BW, solder mass volume/VB and height H1/H2 being such that H1 is larger than H2 (Fig. 2)
- (Fig. 1 and 2; Col. 1, line 22- Col. 2, line 40).

Van Den Brekel et al. fail to teach:

- a) the solder pads being generally circular having respective centers and diameters D, and
- b) H1 and H2 being approximately equal.
- a) Amano et al. teach a substrate having a solder bar/mass (3 in Fig. 2) connecting solder pads/solder bar pad (2 in Fig. 1 and 2) where the solder pads have different configurations/shapes (2c in Fig. 1 and Fig 5A-E) including a generally circular shape having respective center and a diameter and the solder bar pad width being less than

the diameter of the solder pads (2c and 2A respectively in Fig. 5D; Col. 6, line 29; Col. 4-6).

b) Dockerty et al. teach a solder support/bar structure in a flip chip assembly to improve an alignment/spacing between the substrate and a device (Col. 2, line 55) where the flip chip device has solder bars/supports (16/20, 17/20, etc. connecting two or more contact pads 11 in Fig. 3 and 4) having dimensions such that the height and a cross-section of the solder bar/support is uniform between the contact pads including a mid point of the solder bar/support, the height being same as the diameter of the solder ball (Col. 4, lines 50-55; Col. 2-4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the solder pads being generally circular having respective centers and diameters D as taught by Amano et al. and H1 and H2 being approximately equal as taught by Dockerty et al. so that the alignment/spacing between the substrate and the device can be controlled and the solder reflow defects can be reduced in Van Den Brekel et al's device.

Regarding claim 17, Van Den Brekel et al., Amano et al. and Dockerty et al., teach substantially the entire claimed structure as applied to claim 16 above, except the convex-arcuate solder humps/bumps being conventional circular solder bumps having a height H3 where H3 is approximately equal to H1 and H2.

Dockerty et al. further teach the solder support/bar structure in a flip chip assembly where solder balls/bumps on the surface of the substrate/chip have conventional/circular cross-section (11 in Fig. 4 and have uniform height across the from the contact pads along the solder bar/support (Col. 4, lines 50-55; Col. 2-4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate conventional circular solder bumps having a height  $H_3$  where  $H_3$  is approximately equal to  $H_1$  and  $H_2$  as taught by Dockerty et al. so that the spacing between the substrate and the device can be controlled and the solder reflow defects can be reduced in Amano et al. and Van Den Brekel et al's device.

Regarding claims 18 and 19, Van Den Brekel et al., Amano et al. and Dockerty et al., teach substantially the entire claimed structure as applied to claims 16 and 17 above, except the solder bump diameter ( $D_c$ ) and the volume ( $V_c$ ) being such that  $D$  is in a range of  $D_c$ - $2D_c$  and  $VB$  being in a range of  $2V_c$ - $5V_c$  respectively.

The determination of values/range of dimensions such as  $D$ ,  $H_1$ ,  $H_2$ ,  $BW$ ,  $BL$ , solder bump volume/ $VB$ , size/shape, number, spacing, etc. for components including solder pad, solder bar/support, fillet, solder bump, etc., in chip soldering/package and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired spacing, alignment, bonding strength and solder joint integrity and reliability.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to select the solder bump diameter ( $D_c$ ) and the volume ( $V_c$ ) being such that  $D$  is in a range of  $D_c$ - $2D_c$  or  $VB$  being in a range of  $2V_c$ - $5V_c$  so that the spacing between the substrate and the device can be controlled, solder reflow defects

can be reduced and the solder joint integrity/reliability can be improved in Amano et al. Dockerty et al., and Van Den Brekel et al's device.

Regarding claim 20, Dockerty et al., Lee et al. and Thompson teach substantially the entire claimed structure as applied to claim 16 above, except the first substrate being a flip chip IC.

Dockerty et al. further teach the chip/substrate package where the substrate/first substrate is a flip chip IC (3 in Fig. 3 and 4; Col. 4).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first substrate being a flip chip IC as taught by Dockerty et al. so that additional wiring and external connections can be provided on the second substrate in Amano et al. and Van Den Brekel et al's device.

Regarding claims 21 and 22, Van Den Brekel et al., Amano et al. and Dockerty et al., teach substantially the entire claimed structure as applied to claim 16 above, except the difference between H2 and H1 being less than 10% of H2 or 5% of H2 respectively.

The determination of values/range of dimensions such as D, H1, H2, BW, BL, solder bump volume/VB, size/shape, number, spacing, etc. for components including solder pad, solder bar/support, fillet, solder bump, etc., in chip soldering/packaging and interconnection technology art is a subject of routine experimentation and optimization to achieve the desired spacing, alignment, bonding strength and solder joint integrity and reliability.



It would have been obvious to a person of ordinary skill in the art at the time invention was made to select difference between H2 and H1 being less than 10% of H2 or 5% of H2 so that the spacing between the substrate and the device can be controlled, solder reflow defects can be reduced and the solder joint integrity/reliability can be improved in Amano et al. Dockerty et al., and Van Den Brekel et al's device.

### ***Response to Arguments***

5. Applicant's arguments filed on 05-05-03 have been fully considered but they are not persuasive.

A. Applicant contends that low melting temperature (LMT) reflowable solder as recited in claim 16 is the same as the conventional tin/lead eutectic solder.

However, LMT solder comprise a variety of solders having a range of compositions and properties, such solders including tin/bismuth, tin/indium, etc., (see Dockerty et al.: Col. 4, line 65) which have different properties than eutectic tin/lead solder. The specification (pages 1-11) discloses the solder being tin/lead eutectic composition solder and not any other solders having low temperature melting properties.

B. Applicant's arguments with respect to the teachings of Lee et al. Jonaidi and Thompson are moot in view of new ground of rejection.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

07-01-03



TOM THOMAS  
SUPERVISORY PATENT EXAMINER  
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